HIGH Q ON-CHIP PASSIVE COMPONENTS FOR UTSi® CMOS TECHNOLOGY

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ABSTRACT

UTSi (Ultra-Thin Silicon) on insulator technology shows the promise of full integration of digital, analog, RF, and RF matching circuitry on a single chip. It is based on standard VLSI technology. The process features excellent isolation due to the dielectric substrate, high RF performance transistors, and high quality passive elements. This paper presents the performance of the UTSi passive elements. Measurement data for resistors and capacitors are reported, as well as inductors with high Q.

INTRODUCTION

Maturity, low cost, and high levels of integration are the key aspects of silicon CMOS technology. Silicon has obviously dominated digital and mixed-signal applications and is showing signs of taking the place of GaAs technology in RF systems, which presently consist of discrete chip elements. The main concern about Si CMOS technology, especially for RF applications, is the high substrate losses compared to GaAs. Also, aluminum (Al) or aluminum-copper (AlCu) interconnects are typically used, which have higher resistivity than the gold employed in GaAs technology. Also, the metal thickness used with standard bulk Si are also much thinner than GaAs. These factors require the introduction of a version of Si CMOS that offers high performance RF along with high speed, low power digital and mixed-signal capabilities supplemented with integrated high Q passive components. This solution would be ideally on a low loss, nondispersive dielectric substrate that eliminates the parasitics and coupling among the different components located on the same integrated circuit. Of course, the expected solution should also fulfill the low cost requirement for the new customer driven market. UTSi technology has been developed to meet the requirements for system-on-chip solution [1].

High Q passive components are an essential feature of UTSi technology. The passives are manufactured according to standard VLSI design rules. The Al metal thickness is less than 1 μm. However, the insulating sapphire substrate compensates for much of the thin conductor losses at high frequency and allows an efficient optimization of the inductor structures. Also, the RF series resistance for thin metal is less dispersive than the thick metal, since the Al skin depth is larger than the metal thickness at the RF commercial operating frequencies. The quality factor (Q) of spiral inductor on Si by using thick gold metal on high resistivity Si substrate (HRS) [2], multilayer (four levels) of non standard AlCu metal [3], micromachining [4], and coplanar inductor [5], the maximum achievable quality factor was

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about 60% the value obtained on GaAs technology. In this paper, resistors, capacitors, and inductors associated with UTSi technology will be described. A direct algorithm that determines the lumped equivalent circuit elements will be explained. Different types of passive components will be reported and compared.

RESISTOR ON UTSi

There are four types of resistors in UTSi technology, polysilicon/polycide (poly), P^+ silicon, N^+ silicon, and SN. The resistance values are 8 ohm/square, 200 ohm/square, 200 ohm/square and 2000 ohm/square for the poly, N^+, P^+, and SN resistors, respectively. The N^+ and P^+ are the heavily doped source and drain regions in UTSi technology. The SN resistance has lower doping to provide high resistance value per unit area. Moreover, the temperature coefficient (TCR) of the SN resistor is very low (-144 ppm/^{o}C). Table I summarizes the matching results for N^+ and SN resistors at 1.2um and 5um width by 20um long. All median values are close to zero, indicating no significant systematic mismatch between the resistors. All mismatch numbers are about 1% or less. These results show that UTSi technology can deliver resistances that meet the requirements of RFIC design for wireless systems.

CAPACITOR ON UTSi

MOS, interdigital, and double poly capacitances exist on UTSi technology process. The MOS gate and double poly capacitors have 3.3 fF/μm^2 and 1.5 fF/μm^2, respectively. The double poly capacitor, shown in Fig. 1, has the following dimensions: poly1 thickness 0.3 μm, interpoly oxide 0.03 μm, and poly2 thickness 0.3 μm. The distance between poly1 and the substrate is 0.1 μm. The double poly capacitor provides high capacitance per unit area values. Q of 185 at 1 Ghz is measured for 0.41 pF double poly capacitance with series resistance of 2.1 ohm. The 0.51 pF MOS capacitor has lower Q of 35 at 1 GHz as expected. The series resistance associated with the MOS capacitor is 4.9 ohm. Three dimensional interdigital capacitances are also fabricated in UTSi technology to provide moderate capacitance/unit area with high Q.

INDUCTANCE ON UTSi

CMOS UTSi technology, which is based on VLSI technology, with three metal layers of Al metal lines has been used to fabricate several inductors with various number of turns and different number of metal layers, as shown in Fig.2. The isolation oxide thickness between the substrate and the first metal layer is 1 μm, which is roughly the same thickness as conventional CMOS process. The thickness of the Al metal layers are 0.5 μm, 0.5 μm and 0.8 μm for metal #1 (M1), metal #2 (M2), and metal #3 (M3), respectively. The inter-metal dielectrics (IMD's) have 0.8 μm thickness. In UTSi technology, there is no substrate ground, since the wells are eliminated from the process [1]. This makes the metal lines of the UTSi technology in coplanar waveguide configuration in the normal operating conditions.

In this paper, six different configurations of spiral inductors will be reported and studied. All the inductors have M1 as a return ground. Single, double, and triple layer metals spiral inductors with 4.5 and 8.5 turns were developed, M2, M2/M3, and M1/M2/M3, respectively. S-parameters for the single and double layers inductances, with metal width of 10 μm and spacing of 1 μm, were measured using the method described in [3]. The triple layer

inductances, with metal width of 15 μm and spacing of 1.3 μm, were optimized according to the measured structures to provide the target high Q inductance. The lumped element equivalent circuits, shown in Fig. 3, is used to model the spiral inductors. This circuit approximation is derived from the measured S-parameters up to 8 Ghz, since the skin depth for Al metal is 0.9 μm at 9 Ghz. The S-parameters are converted into Y-parameters. The *Q* of the inductor is determined as the ratio of the imaginary part to the real part of the impedance derived from Y_{12} extracted from the two port s-parameters measurement at 2 GHz. In UTSi technology, the losses in the sapphire substrate are negligible. The input and output shunt capacitances effects on the calculated Q at 2 GHz is mostly insignificant. Their effects will be pronounced as frequency increases. In general, the shunt capacitances depend on the layout of the inductance structure in the real circuit.

Table I.a and I.b shows the lumped circuit elements, resonance frequency, and Q for the six spiral inductors under investigation. C_1 and C_2 increase with the number of turns. Their values are approximately the same for the single and double layer inductors with the same number of turns. C_1 and C_2 are not equal which makes S_{11} and S_{22} different. C_f increases with the number turns. The change in the resonance frequency is very small between the single and double metal layers inductance structures. L_s increases with increasing number of turns. The inductance is approximately the same for the single and multi-metal layers inductances with the same number of turns. R_s increases with the number of turns. However, the value of the series resistance for the double layer inductance is almost half of the single layer case with the same number of turns. Although, UTSi technology is based on VLSI process, high Q inductance is achieved relative to traditional Si-based technologies. The measured inductance Qs at 2 Ghz are 4.35 and 6.36 for the double layer inductance of 4 and 8 turns, respectively. For the single layer inductances, Qs equal to 2.5 and 3.5 for the 4.5 and 8.5 turns, respectively. The calculated Q for the optimized triple layers inductances are 10 and 15 for the 4.5 and 8.5 turns, respectively. The improvement in Q is more significant with the large number of turns than the small number of turns inductance. The presented results show that spiral inductances can be optimized by choosing the proper number of turns, metal width, and metal spacing in the operating frequency range of Silicon RFIC. It is obvious that UTSi technology is capable of producing the high Q inductances required for wireless communications systems.

CONCLUSION

UTSi technology shows the promise of full RF, digital, and analog integration due to the unique dielectric substrate. Resistors with a wide range of values, good matching, and low temperature coefficient of resistance are presented. Double poly capacitors with high Q's and excellent voltage coefficient of capacitance are shown. Very high integrated inductor Q's are achieved due to the presence of the insulating substrate. The performance of passive components integrated onto this technology allows for on-chip matching of RF circuits.

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Table 1.a Inductors C1, C2, Cf, and resonance frequency for M1 and M1/M2.

Metal layers	**2**		**1**	
# of turns	**4.5**	**8.5**	**4.5**	**8.5**
C1 (fF)	25	55	25	54
C2 (fF)	19	25	17	26
Cf (fF)	34	46	25	34
Fres (GHz)	13	6.0	14	6.1

Table 1.b Inductors Ls, Rs and Q for M1, M2/M3 and M1/M2/M3.

Metal layers	**3**		**2**		**1**	
Width	15 μm		10 μm		10 μm	
Spacing	1.3 μm		1.0 μm		1.0 μm	
# of turns	**4.5**	**8.5**	**4.5**	**8.5**	**4.5**	**8.5**
Ls (nH)	5.0	19	4.5	17	4.7	18
Rs (ohm)	4.8	11	12	27	23	54
Q@2GHz	10	15	4.4	6.4	2.6	3.5

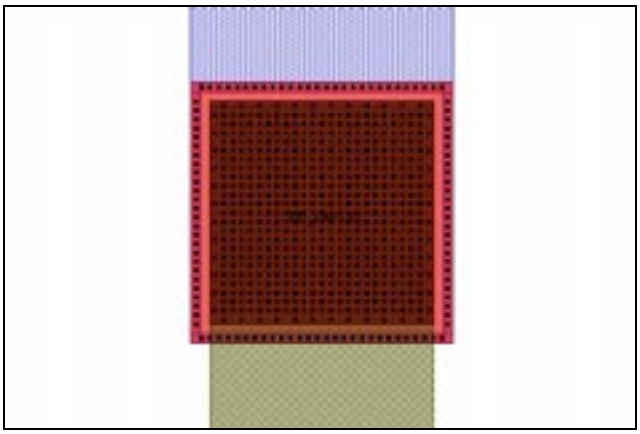

Fig. 1 The double poly capacitor.

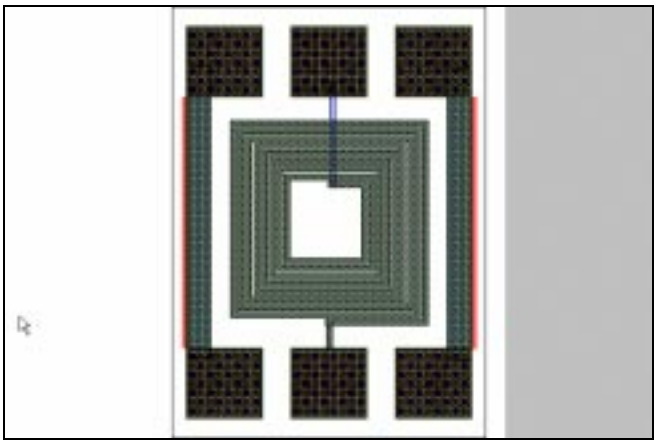

Fig. 2 M2/M3 8 turns spiral inductor.

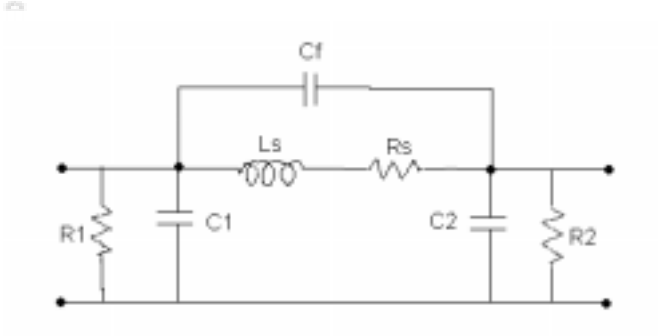

Fig. 3 Lumped equivalent circuit model for spiral inductance.